". . . a data bus connected to a peripheral apparatus and including a plurality of unit data buses, into which the data bus is divided and through each of which data is transferred concurrently;. . .

a bus controller configured to split-control said data bus in unit data buses for said plurality of bus masters by giving a grant signal which grants the use of said data bus in units of the unit data bus requested in unit data buses to said bus masters in accordance with an availability of said data bus in units of the unit data bus, wherein

the request signal and the grant signal indicate identification or number of the unit data bus divided from the data bus."

By way of background, data transfer is controlled in information processing systems by a central processing unit (CPU) and direct memory access controllers (DMACs)for communicating with peripheral devices. The peripheral devices often employ a data bus and an address bus for communicating with the information processing system. Where more than one peripheral device is connected to the bus, it is necessary to employ a bus arbitration scheme for managing the transfer of data between the information processing system and the various peripheral devices. However, in conventional information processing systems, if I/O access occurs for polling processing or the like by the CPU during the DMA data transfer, the DMA data transfer and the I/O access cannot be carried out simultaneously regardless of the fact that only a part of the data bus is necessary for the data transferred by the I/O access. Further, when the I/O access for the polling processing or the like by the CPU occurs during the DMA data transfer, the data bus is not released until a break of the DMA data transfer, thereby stalling CPU functionality.[1]

In light of the above deficiency in the art the present invention is provided. With this object in mind, a brief comparison of the claimed invention in view of the cited reference is believed to be in order.

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[1] Application at pages 1-3.

Kato discloses a high-speed processor system employing a bus arbitration methodology. The high-speed processor system includes a plurality of buses (10), each bus having an independent address bus an independent data bus for achieving data transfer capability. At least one bus master (41) is directly connected to all of the buses by way of a plurality of independent bus interfaces.[2] In operation, a first bus arbitrator arbitrates the access of the first bus for each bus master having issued the first bus request signal and determines which bus master may use the next bus cycle.[3] Since each bus master can use the first bus only while it receives the first bus grant signal, no two bus masters may use the first bus at the same time.[4]

Conversely, Applicant's data transfer control circuit provides a plurality of unit data buses into which the data bus is divided and to each of which data is transferred concurrently. Since the request signal and the grant signal used for bus arbitration by the bus masters and the bus controller indicate identification or the number of the unit data bus divided from the data bus, data transfer is enabled not in units of the data bus, but in units of the unit data bus divided from the data bus which employs one address space. Thus, by specifying the identification or necessary number of the unit data bus, bus utilization and data transfer is enhanced.

As can be appreciated, Kato does not disclose or suggest using a request signal and grant signal for bus arbitration by the bus masters and the bus controller to indicate identification or number of the data bus divided from the data bus, and data transferring units of the unit data bus divided from the data bus which employs one address space, by

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[2] Kato at column 5, line 66 through column 6, line 5.

[3] Kato at column 7, lines 30-33.

[4] Kato at column 14, lines 26-34.

specifying the identification or necessary number of the data bus. Thus, in Kato, for example, data access to DMA and data access to the register containing bus arbitration information cannot be carried out concurrently through one data bus.

Likewise, independent Claims 8 and 15 recite substantially the same limitations as discussed above with reference to Claim 1, as such, these claims and any claims depending therefrom are allowable at least for the same reasons.

Accordingly, Applicant respectfully requests that the rejection of Claims 1-20 under 35 U.S.C. § 102 be withdrawn.

NEW CLAIMS

As new Claims 21-26 recite substantially the same limitations as discussed above, Applicant submits that these claims are likewise allowable over the cited art.

CONCLUSION

Consequently, in view of the foregoing amendment and remarks, it is respectfully submitted that the present application, including Claims 1-20, is patentably distinguished over the prior art, in condition for allowance, and such action is respectfully requested at an early date.

Finally, the attention of the U.S. Patent and Trademark Office is directed to the change of address of Applicants' representative, effective January 6, 2003:

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Please direct all future communications to this new address.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
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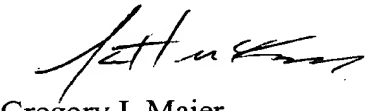

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Serial No: 09/664,856
Amendment Filed on:
5-19-03

IN THE CLAIMS:

1. (Amended) A data transfer control circuit for carrying out data transfer by using a plurality of bus masters, comprising:

a data bus connected to a peripheral apparatus and [composed of] including a plurality of unit data buses [each capable of carrying out data transfer independently], into which the data bus is divided and through each of which data is transferred concurrently;

a plurality of bus masters [each for sending] configured to send a request signal requesting a use of said data bus in [unit] units of the unit data [buses,] bus, and using said data bus in unit data buses requested when a request by means of said request signal is granted; and

a bus controller [for split-controlling] configured to split-control said data bus in unit data buses for said plurality of bus masters by giving a grant signal which grants the use of said data bus in [unit] units of the unit data [buses] bus requested in unit data buses to said bus masters in accordance with an availability of said data bus in [unit] units of the unit data [buses] bus, wherein

the request signal and the grant signal indicate identification or number of the unit data bus divided from the data bus

8. (Amended) An information processing system for carrying out data transfer by using a plurality of bus masters, comprising:

a peripheral apparatus;

a data bus connected to said peripheral apparatus and [composed of] including a plurality of unit data buses [each capable of carrying out data transfer independently], into which the data bus is divided and through each of which data is transferred concurrently;

a plurality of bus masters [each for sending] configured to send a request signal requesting a use of said data bus in [unit] units of the unit data [buses] bus, and using said data bus in unit data buses requested when a request by means of said request signal is granted; and

a bus controller [for split-controlling] configured to split-control said data bus in unit data buses for said plurality of bus masters by giving a grant signal which grants the use of said data bus in [unit] units of the unit data [buses] bus requested in unit data buses to said bus masters in accordance with an availability of said data bus in [unit] units of the unit data [buses] bus, wherein,

the request signal and the grant signal indicate identification or number of the unit data bus divided from the data bus.

15. (Amended) A method of carrying out data transfer by using a plurality of bus masters, comprising [the steps of]:

generating a request signal requesting a use of a data bus in [unit] units of the unit data [buses] bus in each of a plurality of bus masters and sending said each request signal to a bus controller, said data bus being connected to a peripheral apparatus and [composed of] including a plurality of unit data buses [each capable of carrying out data transfer

independently], into which the data bus is divided and through each of which data is transferred concurrently;

sending, in response to said request signal, a grant signal granting the use of said data bus in [unit] units of the unit data [buses] bus requested in unit data buses to said bus master in accordance with an availability of said data bus in [unit] units of the unit data [buses] bus; and

occupying said data bus granted by said grant signal in [unit] units of the unit data [buses] bus, and carrying out data transfer by using the unit data buses thus [occupied.] occupied, wherein

the request signal and the grant signal indicate identification or number of the unit data bus divided from the data bus.

21-26. (New)